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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/459,967	12/13/1999	HISASHI TACHIBANA	450100-02223	1861

20999 7590 02/17/2004

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EXAMINER	
DO, NHAT Q	

ART UNIT	PAPER NUMBER
2663	11

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/459,967	TACHIBANA, HISASHI	
	Examiner	Art Unit	
	Nhat Do	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 10/06/03 have been fully considered but they are not persuasive.

Applicants argue that Vancelette fails to disclose the selection circuit is operable to extract two channels of data simultaneously (Remarks page 6, 1st and 2nd paragraphs).

In reply, Vancelette discloses the selection circuit (the set-top terminal 70 in figure 5) selects the primary channel (primary signal) using PID for the screen displaying (Col. 10, lines 21-35; the selection circuit (the set-top terminal 70 in figure 5) also selects the alternate channel (alternate signal) using appropriate PID for the screen displayer (Col. 10, line 57-col. 11, line 5). Moreover, Vancelette also discloses the viewer has the capable of viewing both the primary and alternate signals (primary and alternate channels) in a split-screen or picture in picture format (Col. 4, lines 41-48). Therefore the examiner is in the position the selection circuit (the set-top terminal 70 in figure 5) is operable to extract two channels of data simultaneously when the viewer views both primary and alternate signals.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. patent No. 6,434,146 to Movshovich et al in view of U.S. Patent No. 5,894,320 to Vancelette.

Regarding to claim 1, Movshovich et al disclose a data processing circuit comprising:

The front-end interface 104 receives plurality-of-channels input (Fig. 1);

The selection circuit in figure 5 having:

The channel identification data extracting circuit 354 for extracting channel identification data regarding a selected channel in input packet data (fig. 5; col. 8, lines 36-67);

The comparison circuit 372 for comparing the extracted channel identification data with channel specifying data regarding a predetermined selected channel (Fig. 5; col. 9, lines 18-27);

The packet data validity instruction signal generation circuit 380 for outputting a packet data validity instruction signal indicating whether the packet data is valid or not based on the comparison result (Fig. 5, 6; col. 10, lines 1-47);

The selection circuit 400 provides input packet data to transmission path when packet data validity instruction signal is valid (Col. 10, line 28-67).

Movshovich et al fail to disclose the selection circuit selects two channels simultaneously. Vancelette disclose a processing circuit comprising a set-top terminal 70 (selection circuit) in figure 5 that extracts a primary channel, and alternate channel simultaneously (Col. 4, lines 42-48; col. Col. 10, line 39-col. 11, line 11). A skilled

artisan would have been motivated to modify the selection circuit in Movshovich et al system so that it selects two channels at the same time as the set-top terminal 70 in Vancelette in order to allow the viewers to watch two programs from different provider as taught by Vancelette. Therefore, it would have been obvious to a person having ordinary skill in the art by the time the invention was made to have the selection circuit of Movshovich et al designed for extracting two channels simultaneously.

Regarding to claim 2, Movshovich et al disclose the channel identification data extraction circuit 354 receives a timing signal 356 for specifying an input timing of the packet data and extracts the channel identification data based on the input timing (Col. 8, lines 40-67).

Regarding to claim 3, Movshovich et al disclose the transmission circuit transmits insert data (gap signal) when there is no data for transmitting (Col. 13, lines 5-7; lines 47-56). Movshovich et al also disclose the transmission circuit receives data when data validity instruction signal is valid (Col. 10, lines 40-54). Therefore, the examiner is in the position the transmission circuit transmits the insert data (gap signal) when data validity instruction signal is invalid (because there is data coming).

Regarding to claim 4, Movshovich et al disclose the insert data (gap signal) is information data regarding the selected channel because the signal indicate the channel has no data to send.

Regarding to claim 5, Movshovich et al disclose the data processing circuit further comprises a memory circuit (PID table) for storing the channel specifying data (Col. 7, lines 63-65).

Regarding to claim 6, Movshovich et al disclose the memory circuit (PID table) is updated by the computer (processor) 216 (Col. 7, lines 65-67; col. 8, lines 39-41), the examiner understands that the computer 216 is used for writing channel specifying data because the examiner interprets "update" by writing new and deleting unused information.

Regarding to claim 7, Movshovich et al disclose a transmission packet data memory circuit 428 for storing packet data to be transmitted to the data transmission path (Fig. 6; col. 12, lines 21-25).

Wherein the transmission circuit 400 selects the input data and writes it to a transmission packet data memory circuit 428 when the packet data validity instruction signal indicates validity (Fig. 6; col. 10, lines 38-54; col. 12, lines 21-25).

Regarding to claim 8, Movshovich et al fail to disclose explicitly the transmission circuit transmits data at predetermined intervals. However, Movshovich et al disclose the circuit transmits data at the same fixed rate of input data (Col. 12, lines 45-49; col. 13, lines 23-30). Movshovich et al also disclose the transmission circuit transmits data in fixed length packet (Fig. 7). It would have been obvious to a person having ordinary skill in the art by the time the invention was made to modify the transmission circuit in the system taught by Movshovich et al so that it transmits data at predetermined intervals depending the capacity of the transmitter. A skilled artisan would have been motivated to so in order to keep the circuit transmits data at fixed rate of input data as taught by Movshovich et al

Regarding to claim 9, Movshovich et al disclose using IEEE 1394 standard, which uses serial bus (Col. 12, line 65-col.13, line 5).

Regarding to claim 10, Movshovich et al disclose the device comprises an IEEE 1394 interface (Col. 12, lines 34-49).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhat Do whose telephone number is (703) 305-5743. The examiner can normally be reached on 9:00 AM - 6:00 PM (Monday-Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (703) 308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nhat Do
Examiner
Art Unit 2663

ND

February 9, 2004.

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 2/12/04